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PTO/SB/05 (6-95) (modified)


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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

0002/PTO Rev. 6/95 NEW UTILITY PATENT APPLICATION TRANSMITTAL <i>(to be used for new applications only)</i>	U.S. Department of Commerce Patent and Trademark Office	Attorney Docket Number 2723 First Named Inventor Reena Premi Total Pages in this Submission 59
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APPLICATION ELEMENTS	ACCOMPANYING APPLICATION PARTS
<p><i>Notice. Checklist items mentioned under Application Elements section construct a new utility patent application. Please refer to MPEP Sections 506, 601 (37 CFR 1.77, 1.53, 35 USC 111, 112, 113) for detailed explanation regarding completeness of an original patent application.</i></p>	
<p>1. <input checked="" type="checkbox"/> Fee Transmittal Form (in duplicate) <input checked="" type="checkbox"/> Check Enclosed</p>	<p>5. <input type="checkbox"/> FWC Application Filing Papers under 37 CFR § 1.62</p>
<p>2. Specification</p> <p><input checked="" type="checkbox"/> Title of the Invention</p> <p><input type="checkbox"/> Cross Reference(s) to Related Case(s)</p> <p><input type="checkbox"/> Statement Regarding Federally-sponsored Research/Development</p> <p><input checked="" type="checkbox"/> Background of the Invention</p> <p><input checked="" type="checkbox"/> Brief Summary of the Invention</p> <p><input checked="" type="checkbox"/> Brief Description of the Drawing(s)</p> <p><input checked="" type="checkbox"/> Detailed Description</p> <p><input checked="" type="checkbox"/> Claim or Claims</p> <p><input checked="" type="checkbox"/> Abstract of the Disclosure</p> <p><input type="checkbox"/> Appendix</p>	<p>6. <input type="checkbox"/> Application Filing Papers Under 37 CFR § 1.60</p> <p>7. <input type="checkbox"/> Assignment & PTO-1595</p> <p>8. <input type="checkbox"/> Certified Copy of Priority Document(s) <i>(if foreign priority is claimed)</i></p> <p>9. <input type="checkbox"/> Information Disclosure Statement & PTO-1449</p>
<p>3. <input checked="" type="checkbox"/> Drawing(s) (<i>when necessary per 35 USC 113</i>)</p>	<p>10. <input type="checkbox"/> Copies of IDS Citation(s)</p>
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Signature:			
Attorney/Reg No.:	Greg T. Sueoka, 33,800	Dated:	November 13, 1997

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Application Number			Class		Independent Claims	
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0002/PTO(modified) Rev. 10/95	U.S. Department of Commerce Patent and Trademark Office	Complete if Known
FEE TRANSMITTAL		Application Number Not yet assigned
		Filing Date On Even Date Herewith
		First Named Inventor Reena Premi
		Group Art Unit Unknown
		Examiner Name Unknown
		Attorney Docket Number 2723
TOTAL AMOUNT OF PAYMENT Subtotal (1) + Subtotal (2) + Subtotal (3) = (\$1,076.00)		

METHOD OF PAYMENT	FEE CALCULATION (continued)																																																																																								
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ADDITIONAL FEES <table style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left;">Large Entity Fee Code/Fee</th> <th style="text-align: left;">Small Entity Fee Code/Fee</th> <th style="text-align: left;">Fee Description</th> <th style="text-align: right;">Fee Due</th> </tr> </thead> <tbody> <tr><td>105/\$130</td><td>205/\$65</td><td>Surcharge - late filing fee or oath</td><td style="text-align: right;">[]</td></tr> <tr><td>127/\$50</td><td>227/\$25</td><td>Surcharge-late provisional filing fee or cover sheet</td><td style="text-align: right;">[]</td></tr> <tr><td>147/\$2,520</td><td>147/\$2,520</td><td>For filing a request for reexamination</td><td style="text-align: right;">[]</td></tr> <tr><td>115/\$110</td><td>215/\$55</td><td>Extension for response within first month</td><td style="text-align: right;">[]</td></tr> <tr><td>116/\$400</td><td>216/\$200</td><td>Extension for response within second month</td><td style="text-align: right;">[]</td></tr> <tr><td>117/\$950</td><td>217/\$475</td><td>Extension for response within third month</td><td style="text-align: right;">[]</td></tr> <tr><td>118/\$1,510</td><td>218/\$755</td><td>Extension for response within fourth month</td><td style="text-align: right;">[]</td></tr> <tr><td>119/\$310</td><td>219/\$155</td><td>Notice of Appeal</td><td style="text-align: right;">[]</td></tr> <tr><td>140/\$110</td><td>240/\$55</td><td>Petition to revive unavoidably abandoned application</td><td style="text-align: right;">[]</td></tr> <tr><td>141/\$1,320</td><td>241/\$660</td><td>Petition to revive unintentionally abandoned application</td><td style="text-align: right;">[]</td></tr> <tr><td>142/\$1,320</td><td>242/\$660</td><td>Utility Issue Fee (Or Reissue)</td><td style="text-align: right;">[]</td></tr> <tr><td>143/\$450</td><td>243/\$225</td><td>Design Issue Fee</td><td style="text-align: right;">[]</td></tr> <tr><td>122/\$130</td><td>122/\$130</td><td>Petitions to the Commissioner</td><td style="text-align: right;">[]</td></tr> <tr><td>123/\$50</td><td>123/\$50</td><td>Petitions related to provisional applications</td><td style="text-align: right;">[]</td></tr> <tr><td>126/\$240</td><td>126/\$240</td><td>Submission of Information Disclosure Statement</td><td style="text-align: right;">[]</td></tr> <tr><td>581/\$40</td><td>581/\$40</td><td>Recording each patent assignment per property (times number of properties)</td><td style="text-align: right;">40</td></tr> <tr><td>146/\$790</td><td>246/\$395</td><td>Filing a submission after final rejection (37 CFR 1.129(a))</td><td style="text-align: right;">[]</td></tr> <tr><td>149/\$790</td><td>249/\$395</td><td>For each additional invention to be examined (37 CFR 1.129(b))</td><td style="text-align: right;">[]</td></tr> <tr><td colspan="3">Other fee (specify):</td><td style="text-align: right;">[]</td></tr> <tr><td colspan="3">Other fee (specify):</td><td style="text-align: right;">[]</td></tr> <tr> <td colspan="3" style="text-align: right;">SUBTOTAL (3)</td> <td style="text-align: right;">(\$40)</td> </tr> </tbody> </table>	Large Entity Fee Code/Fee	Small Entity Fee Code/Fee	Fee Description	Fee Due	105/\$130	205/\$65	Surcharge - late filing fee or oath	[]	127/\$50	227/\$25	Surcharge-late provisional filing fee or cover sheet	[]	147/\$2,520	147/\$2,520	For filing a request for reexamination	[]	115/\$110	215/\$55	Extension for response within first month	[]	116/\$400	216/\$200	Extension for response within second month	[]	117/\$950	217/\$475	Extension for response within third month	[]	118/\$1,510	218/\$755	Extension for response within fourth month	[]	119/\$310	219/\$155	Notice of Appeal	[]	140/\$110	240/\$55	Petition to revive unavoidably abandoned application	[]	141/\$1,320	241/\$660	Petition to revive unintentionally abandoned application	[]	142/\$1,320	242/\$660	Utility Issue Fee (Or Reissue)	[]	143/\$450	243/\$225	Design Issue Fee	[]	122/\$130	122/\$130	Petitions to the Commissioner	[]	123/\$50	123/\$50	Petitions related to provisional applications	[]	126/\$240	126/\$240	Submission of Information Disclosure Statement	[]	581/\$40	581/\$40	Recording each patent assignment per property (times number of properties)	40	146/\$790	246/\$395	Filing a submission after final rejection (37 CFR 1.129(a))	[]	149/\$790	249/\$395	For each additional invention to be examined (37 CFR 1.129(b))	[]	Other fee (specify):			[]	Other fee (specify):			[]	SUBTOTAL (3)			(\$40)
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1 SYSTEM AND METHODS FOR 2-TAP / 3-TAP FLICKER FILTERING

2
3 Inventors: Reena Premi
4 William S. Herz
5 Ignatius B. Tjandrasuwita
6

7 BACKGROUND OF THE INVENTION

8 1. Field of the Invention

9 This invention relates generally to processing of computer
10 graphics for display on a television, and more particularly, to
11 flicker filtering for computer graphics.

12 2. Description of the Related Art

13 As the result of the continuous development of new
14 technologies, the distinction between computers, in particular
15 computer monitors, and televisions is becoming increasingly
16 blurred. In other words, the computer and television industries
17 are converging. For example, computer networks such as the
18 Internet and the World Wide Web used to be almost exclusively a
19 computer phenomena. Now, however, televisions may also be used
20 to access these networks. As another example, broadcast
21 entertainment used to belong squarely in the television domain.
22 Now, however, many service providers are offering entertainment
23 to computer users through computer networks. As a result of this
24 convergence, there is a need to display computer graphics
25 originally intended for computers on televisions.

26 Televisions and computers, however, generally use
27 incompatible graphics formats. For example, many formats for

1 computer monitors and flat panel displays are non-interlaced. In
2 other words, the entire frame of computer graphics is updated at
3 once. In contrast, many common television formats are
4 interlaced, meaning that the frame is divided into odd and even
5 fields and only one field or half the frame is updated at a time.

6 As a result, in order to display computer graphics on a
7 television, the computer graphics often must be converted from a
8 non-interlaced to an interlaced format. This conversion
9 typically includes dropping lines of the display. However, this
10 introduces undesirable visual effects as a result of the
11 conversion from a non-interlaced to an interlaced format.

12 In addition to the conversion process, the prior art also
13 performs flicker filtering to improve the image quality. Two
14 common types of flicker filtering are 2-tap and 3-tap filtering,
15 in which either two or three non-interlaced lines are combined to
16 form each interlaced line. The prior art has attempted to
17 accomplish flicker filtering by dropping lines in both even and
18 odd fields to vertically make the non-interlaced image match the
19 scans line common for interlaced displays.

20 However, there are two problems with the prior art approach.
21 First, the prior art requires that flicker filtering and the
22 conversion be performed serially, one after the other. Moreover,
23 each process, flicker filtering and the conversion, requires its
24 own hardware or a general purpose graphics processor with
25 software to perform each process. Furthermore, the prior art
26 does not provide a way to perform both 2-tap and 3-tap flicker
27 filtering.

1 Thus, there is a need for approaches with the capability of
2 implementing both 2-tap and 3-tap filtering. In addition, there
3 is a need to perform these operations while minimizing hardware
4 requirements.

6 SUMMARY OF THE INVENTION

7 In accordance with the present invention, a device which can
8 perform both 2-tap and 3-tap flicker filtering of non-interlaced
9 lines of computer graphics data to form interlaced lines includes
10 a data packer, a data unpacker, and a filter circuit.

11 The filter circuit receives non-interlaced lines from a
12 computer graphics source and also receives lines temporarily
13 stored in two line buffers. The filter circuit filters the
14 received lines to form filtered lines. The data packer converts
15 the filtered lines to a format suitable for the line buffers and
16 then writes them to the line buffers. The data unpacker reads
17 the lines stored in the line buffers and converts them to a
18 format suitable for the filter circuit. The read lines are
19 either sent to the filter circuit for further filtering or are
20 outputted to be displayed. Both 2-tap and 3-tap flicker
21 filtering can be accomplished by varying the order and/or number
22 of read, write, and filtering operations.

23 The present invention is particularly advantageous because
24 both 2-tap and 3-tap flicker filtering may be accomplished by the
25 same hardware. Moreover, the hardware is simplified since the
26 same basic functions of reading, writing, and filtering are used
27 to accomplish both 2-tap and 3-tap flicker filtering.

BRIEF DESCRIPTION OF THE DRAWING

The invention has other advantages and features which will be more readily apparent from the following detailed description of the invention and the appended claims, when taken in conjunction with the accompanying drawing, in which:

Figure 1 is a block diagram of a system including the present invention;

Figure 2 is a block diagram of a preferred embodiment of the flicker filter device 104 of Figure 1, used to illustrate data flow through the device;

Figure 3A is a block diagram of a preferred embodiment of the flicker filter device 104 of FIGS. 1 and 2;

Figure 3B is a block diagram of a second alternate embodiment of the flicker filter device 104;

Figures 4A and 4B are timing diagrams illustrating a method for 2-tap flicker filtering, utilizing the flicker filter device 104 of Figure 3;

Figures 5A and 5B are timing diagrams illustrating a method for 3-tap flicker filtering, utilizing the flicker filter device 104 of Figure 3;

Figures 6A and 6B are timing diagrams illustrating a second method for 3-tap flicker filtering, utilizing the flicker filter device 104 of Figure 3;

Figures 7A and 7B are timing diagrams illustrating a third method for 3-tap flicker filtering, utilizing the flicker filter device 104 of Figure 3; and

Figure 8 is a timing diagram illustrating the production of output control signals from input control signals, utilizing the flicker filter device 360 of Figure 3B.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIGURE 1 is a block diagram of a system 100 including the present invention. The system 100 includes a data source 102, a flicker filter device 104, a display encoder 106, and two line buffers 108 and 110. The data source 102 is coupled to send input data and an input control signal to the flicker filter device 104 on lines 112 and 114, respectively. Those skilled in the art will realize that the flicker filter device 104 could also receive and process many input data and respective control signals. The flicker filter device 104 is coupled to send output data and an output control signal to the display encoder 106 on lines 116 and 118, respectively. The flicker filter device 104 is also coupled to write and read data to and from the line buffers 108 and 110 on lines 120, 122, 124, and 126, respectively. The read/write operations are controlled by control signals sent from the flicker filter device 104 to the line buffers 108 and 110 on lines 128 and 130, respectively.

The data source 102 provides computer graphics in non-interlaced form and corresponding control signals to the flicker filter device 104. In one embodiment, the data source 102 is a Streams processor or other similar graphics engine, specifically a CRT controller. In an exemplary embodiment, the data source 102 is a Trio 64V+ or ViRGE graphics controller chip made by S3

1 Incorporated of Santa Clara, California. In a preferred
2 embodiment, the data source 102 is a MUX that may select from a
3 number of different data sources, including Streams Processors.
4 In a preferred embodiment, the input data from the data source
5 102 on line 112 is digital data in RGB format.

6 The flicker filter device 104 receives the non-interlaced
7 input data on line 112 and flicker filters the data to produce an
8 interlaced output data on line 116. The device 104 also
9 generates the corresponding output control signal on line 118.
10 In a preferred embodiment, the flicker filter device 104 includes
11 four modes of operation. First, in the 2-tap filter mode, the
12 flicker filter device 104 combines two lines of non-interlaced
13 input data to produce each line of interlaced output data.
14 Second, in the 3-tap filter mode, the flicker filter device 104
15 combines three lines of non-interlaced input data to produce each
16 line of interlaced output data. Third, in the no filter mode,
17 the flicker filter device 104 receives non-interlaced data on
18 line 112 passes it through to the display encoder 106 via line
19 116 without any flicker filtering. Fourth, in a convert only
20 mode, the flicker filter device 104 receives non-interlaced data
21 and converts it from non-interlaced to interlaced, and then it is
22 passed through to the display encoder 106 via line 116 without
23 any flicker filtering.

24 The display encoder 106 receives the interlaced output data
25 on line 116 and provides a source of interlaced data for a
26 display device (not shown in Figure 1). In some embodiments, the
27 display encoder 106 may convert the format of the incoming data

1 to a format more suitable for the display device. For example,
2 in a preferred embodiment, the display device is a television,
3 and the display encoder 106 is a TV encoder. The TV encoder 106
4 may convert the received data on line 116 from a digital to an
5 analog format and/or from a discrete time to a continuous time
6 signal and/or between various color formats.

7 The line buffers 108 and 110 are utilized during flicker
8 filtering. In a preferred embodiment, only one of the line
9 buffers 108 or 110 is used for 2-tap filtering; while both
10 buffers 108 and 110 are used for 3-tap filtering.

11 In a preferred embodiment, the line buffers 108 and 110 are
12 multi-purpose static RAM which can also be used for other
13 purposes. For example, if the flicker filter device 104 is in 2-
14 tap mode and buffer 108 is used for the 2-tap filtering, then
15 buffer 110 may be used for other, perhaps completely unrelated,
16 purposes. As a specific example, in a preferred embodiment, the
17 data source 102 is a streams processor and line buffer 110 is
18 shared with the streams processor. In 2-tap mode, the streams
19 processor may then use the line buffer 110 to vertically
20 interpolate a secondary stream. In no filter mode, both line
21 buffers 108 and 110 may be used for other purposes, such as
22 supporting a second video stream for video conferencing.

23 Figure 2 is a block diagram of a preferred embodiment of the
24 flicker filter device 104 of Figure 1, used to illustrate data
25 flow through the device. The flicker filter device 104 includes
26 a filter circuit 200, a data packer 202, and a data unpacker 204.
27 All of the lines shown in Figure 2 are data lines.

1 The filter circuit 200 has two inputs and one output. A
 2 first input is adapted to receive input data in an external
 3 format on line 112A; the second input is coupled to receive data
 4 from the data unpacker 204 on line 220. The output is coupled to
 5 send data to the data packer 202 on line 222. The filter circuit
 6 200 combines the two input data streams, each of which typically
 7 represents a line of computer graphics, into a single filtered
 8 data line which is output to the data packer 202. In a preferred
 9 embodiment, the filter circuit 200 forms a weighted sum of the
 10 two input lines. In other words, each of the input lines is
 11 multiplied by a constant and the two products then summed to form
 12 the filtered line. In other embodiments, the filter circuit 200
 13 may combine more than two data streams into a single filtered
 14 data line and/or may receive more than one data stream on either
 15 line 112A or 220. For example, the filter circuit 200 may use a
 16 standard filter such as where the first line is multiplied by f
 17 and the second line is multiplied by $(1-f)$, where $0 \leq f \leq 1$.
 18 Still more particularly, such an exemplary filter is given by a
 19 using a pixel from row 1 (Row 1) and a pixel from row 2 (Row 2)
 20 in the equation:

$$\frac{(\text{Row 1} * f)}{16} + \frac{(\text{Row 2} * (1-f))}{16}$$

23 In this example, the pixels are each 8 bits while f is 4
 24 bits. Each numerator is therefore 12 bits. Dividing by 16
 25 reduces the result to 8 bits.

26 The data packer 202 is adapted to write data lines to the
 27 line buffers 108 and 110 via lines 120 and 124. The data packer

1 202 receives the filtered line from the filter circuit 200,
2 converts the filtered line from its external format to an
3 internal format, and then writes the line to one of the line
4 buffers 108 or 110.

5 The terms "internal" and "external" are with respect to the
6 line buffers 108 and 110. The "internal format" is the format
7 used in storing data to the line buffers 108 and 110; while the
8 "external format" is the one used in processing data in the
9 filter circuit 200.

10 In a preferred embodiment, the "external format" is the
11 4:4:4 signed YCrCb format; while the "internal format" may be
12 either the 4:2:2 or the 4:1:1 YCrCb format. The YCrCb format is
13 advantageous because many filters rely heavily on the luminance
14 value, which is the Y in YCrCb. The 4:2:2 and 4:1:1 formats are
15 shorter than the 4:4:4 format, thus allowing the use of smaller
16 line buffers 108 and 110 or, alternatively, allowing more complex
17 filtering to be accomplished with the same size line buffers.
18 For example, data that requires 24 bits per pixel (bpp) in 4:4:4
19 format would require 16 bpp in 4:2:2 format and 12 bpp in 4:1:1
20 format. The conversion of the data by the data packer 202 from
21 4:4:4 YCrCb format to 4:2:2 or 4:1:1 YCrCb format may be done
22 using any one of several circuits and methods well known in the
23 art.

24 The data unpacker 204 is adapted to read data lines from the
25 line buffers 108, 110 via lines 122, 126, respectively. The data
26 unpacker 204 receives the data line from the line buffer 108 or
27 110, converts the line from internal to external format, and then

1 either sends the line to the filter circuit 200 for further
2 filtering or outputs the data line on line 116A. The data
3 unpacker 204 converts the data from 4:2:2 or 4:1:1 YCrCb format
4 to 4:4:4 YCrCb format using any one of the conventional circuits
5 or methods well known in the art.

6 General operation of the flicker filter device 104 occurs as
7 follows. The line buffers 108 and/or 110 hold intermediate
8 results. The data unpacker 204 reads these intermediate results
9 from the line buffers 108 and 110. If the intermediate result is
10 a completed interlaced line, then it is output on line 116A. If
11 it is not a completed interlaced line, then the filter circuit
12 200 combines the intermediate results with an incoming non-
13 interlaced line received on line 112A. The new intermediate
14 result is then written to the line buffers 108 and 110 by data
15 packer 202, and the process is repeated.

16 In an alternate embodiment, the data packer 202 is also
17 adapted to receive input data in an external format on line 112A,
18 thus allowing the writing of such data directly to the line
19 buffers 108 and 110 without first requiring a pass through the
20 filter circuit 200.

21 Figure 3A is a detailed block diagram of a preferred
22 embodiment of the flicker filter device 104 of FIGS. 1 and 2. In
23 addition to the components shown in Figure 2, the flicker filter
24 device 104 further includes a line buffer write control circuit
25 302, a line buffer read control circuit 304, an input register
26 306, a color space converter 308, an output control circuit 310,
27 and a clock circuit 312. Before describing how the various

components are coupled, it will be useful to describe the various signals received and sent by the flicker filter device 104.

The input data on line 112 includes 24 bits of RGB data, denoted by FID[23:0].

The input control signal on line 114 includes control signals for controlling operation of the flicker filter device 104 and control signals for controlling display of the input data. The former include the signals shown in Table 1 below; while the latter are denoted by "Controls" in Figure 3A and are summarized in Table 2.

Table 1: Input Control Signals for Controlling the Flicker Filter Device 104

Input Control Signal	Function
SR70[3:2]	Determines the internal format.
SR80-88[8:0]; SR72[6]	Controls and coefficients for the color space converter 308.
SR70[5,1]; SR71-SR77	Controls the filter circuit 200.
SR70[4]	Controls the output control circuit 310.
CR3D[0]	Enables the flicker filter device 104.
SR70[0]	Enables flicker filtering.

Table 2: Input Control Signals for Controlling Display of Input Data

Input Control Signal	Function
FIDCLK	Dot Clock
FIHSYNC	Horizontal Sync
FIVSYNC	Vertical Sync
FIHDE	Horizontal Display Enable
FIVDE	Vertical Display Enable
FIODDF	Indicates whether odd field or even field is to be produced.
FISSDE	Indicates the location of secondary stream data
FIHBLANK	Horizontal Blanking
FIVBLANK	Vertical Blanking

The output data on line 116 includes 24 bits of 4:4:4 YCrCb data, denoted by FOD[23:0].

The output control signal on line 118 includes the signals shown in Table 3 below.

Table 3: Output Control Signals

Output Control Signal	Function
FODCLK	Dot Clock
FOHSYNC	Horizontal Sync
FOVSYNC	Vertical Sync

The line buffers 108 and 110 can store 720 16-bit pixels or 900 12-bit pixels in the preferred embodiment of Figure 3A. Data is written to or read from the line buffers 108 and 110 in 128 bit chunks, as denoted by signals LB1DW[127:0], LB1DR[127:0], LB2DW[127:0], and LB2DR[127:0].

Line buffer 108 includes two read pointers and one write pointer. The control signal for line buffer 108 on line 128 includes the signals shown in Table 4 below.

Table 4: Control Signals for Line Buffer 108

Control Signal	Function
LB1RD	Read pulse for first read pointer
LB1RD1	Read pulse for second read pointer
LB1WR	Write pulse
LB1RDSEL	Selects between first and second read pointers

LB1RST	Reset first read pointer and write pointer.
LB1RST1	Reset second read pointer.

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Line buffer 110 includes one read pointer and one write pointer. The control signal for line buffer 110 on line 130 includes LB2RD, a read pulse; LB2WR, a write pulse; and LB2RST, a reset for the read and write pointers.

The couplings and basic functions of each of the components in the flicker filter device 104 will now be described.

The clock circuit 312 is adapted to receive the input clock FIDCLK and various other input control signals on line 114 and outputs two clocks: FICLK and FFCLK. More specifically, FIDCLK is inverted and then gated with CR3D[0] (circuit enable), and SR70[0] (flicker filter enable), to generate FICLK, which latches input data and input control signals into the input register 306 and also clocks the color space converter 308. In turn, FICLK is inverted and gated with SR70[0] to generate FFCLK, which clocks the rest of the flicker filter device 104. The skew from FIDCLK to FICLK and the skew from FICLK to FFCLK each is preferably less than half of the minimum clock period.

The input register 306 is adapted to receive the input data on line 112 and Controls on line 114, and is also coupled to receive clock FICLK from the clock circuit 312. The register 306 latches the input data and input control signals on the rising

1 edge of FICLK and then outputs the latched Controls and RGB data,
2 now denoted as FFD[23:0].

3 The color space converter 308 is coupled to receive Controls
4 and RGB data FFD[23:0] from input register 306 and is also
5 coupled to receive FICLK from the clock circuit 312 for clocking
6 purposes. The color space converter 308 is also adapted to
7 receive various other input control signals on line 114. The
8 color space converter 308 performs initial color processing on
9 the input data, partially in response to the control signals
10 received on line 114. More specifically, the color space
11 converter 308 converts the input data from RGB format to 4:4:4
12 signed YCrCb format, the external format. The color space
13 converter 308 may also perform other initial processing, such as
14 color adjustments or chroma filtering. In a preferred
15 embodiment, the color space converter 308 includes a 9-tap chroma
16 filter (not shown) that performs chroma filtering on the output
17 from the color spaced converter. Preferably, the chroma filter
18 uses coefficients of {3, 6, 8, 10, 10, 10, 8, 6, 3}, and scales
19 by 1/64. The processed data, now in YCrCb format, is output on
20 line 112A. The corresponding Controls are also output by the
21 color space converter 308.

22 The filter circuit 200 is coupled to receive Controls and
23 the YCrCb data from the color space converter 308. The filter
24 circuit 200 is also coupled to receive data from the data
25 unpacker 204 on line 220. The filter circuit 200 is further
26 coupled to receive FFCLK from the clock circuit 312 on line 115
27 and adapted to receive various input control signals SR70[5,1]

1 and SR71-SR77 on line 114. As described previously, the filter
2 circuit 200 combines the received input data streams into a
3 single filtered data line which is output to the data packer 202
4 on line 222. Although Figure 3A only depicts two lines 112A and
5 220 for receiving data to be filtered, this depiction is for
6 purposes of clarity in Figure 3A. The filter circuit 200 is not
7 limited to combining two data streams at a time. The filtering
8 is controlled by the various received control signals and clocked
9 by FFCLK.

10 The data packer 202 is coupled to receive the filtered data
11 from the filter circuit 200 on line 222. The data packer 202 is
12 also coupled to receive data in the external format, 4:4:4 YCrCb
13 format in this embodiment, directly from the color space
14 converter 308 on line 112A. The data packer 202 is further
15 coupled to receive control signals from the write control circuit
16 302, adapted to receive input control signals on line 114, and
17 coupled to receive FFCLK from the clock circuit 312. As
18 described previously, the data packer 202 converts received data
19 lines from the external format to an internal format, and then
20 writes the re-formatted line to one of the line buffers 108 or
21 110 via lines 120 or 124.

22 The line buffer write control circuit 302 controls the
23 writing of data from the data packer 202 to the line buffers 108
24 or 110. More specifically, the write control circuit 302 is
25 coupled to receive Controls from the color space converter 308
26 and FFCLK from the clock circuit 312, and is adapted to receive
27 input control signals on line 114. In response to these inputs,

1 the write control circuit 302 generates control signals for the
2 data packer 202 and write control signals for line buffers 108
3 and 110 on lines 128 and 130, respectively.

4 The data unpacker 204 is adapted to receive data lines from
5 the line buffers 108 and 110 via lines 122 and 126. The data
6 unpacker 204 is further coupled to receive control signals from
7 the read control circuit 304 and adapted to receive input control
8 signals on line 114. As described previously, the data unpacker
9 204 converts received lines from internal to external format, and
10 then either sends the line to the filter circuit 200 on line 220
11 for further filtering or outputs the data line on line 116A.

12 The line buffer read control circuit 306 controls the
13 reading of data from the line buffers 108 or 110 to the data
14 unpacker 204. More specifically, the read control circuit 304 is
15 coupled to receive Controls from the color space converter 308
16 and FFCLK from the clock circuit 312, and is adapted to receive
17 input control signals on line 114. In response to these inputs,
18 the read control circuit 304 generates control signals for the
19 data unpacker 204 and read control signals for line buffers 108
20 and 110 on lines 128 and 130, respectively.

21 Finally, the output control circuit 310 is coupled to
22 receive data from the data unpacker 204 on line 116A or from the
23 color space converter 308 on line 112A. The output control
24 circuit 310 also is coupled to receive control signals from the
25 color space converter 308, coupled to receive FICLK and FFCLK
26 from the clock circuit 312, and adapted to receive input control
27 signals on line 114. The output control circuit 310 sends output

1 data, denoted FOD[23:0], to the display encoder 106 of Figure 1
2 on line 116. The output control circuit 310 also converts the
3 input Controls to output control signals appropriate for the
4 output data. The output control signals are transmitted to the
5 display encoder 106 on line 118.

6 The above components were described in the context of
7 converting non-interlaced input data to interlaced output data.
8 The flicker filter device 104, however, need not always implement
9 flicker filtering. For example, the flicker filter device 104
10 may only perform conversion of the data from non-interlaced to
11 interlaced without flicker filtering by setting the value of f to
12 one. For example, flicker filtering may be disabled by not
13 asserting SR70[0] independent of whether conversion is done.
14 Then, the output data provided by the output control circuit 310
15 will be the unfiltered data received from the color space
16 converter 308 on line 112A, and the output clock FODCLK will be
17 FICLK. In contrast, if flicker filtering is enabled, then the
18 output data will be data from the data unpacker 204 on line 116A
19 and the output clock FODCLK will be FFCLK.

20 Referring now to Figure 3B, a second embodiment 360 of the
21 flicker filter device 104 is shown. The second embodiment 360
22 preferably comprises a color space converter 350, a 9-tap chroma
23 filter 352, a plurality of multiplexers 356, 358, a filter and
24 aperture correction circuitry 354, and other control circuitry
25 370, 372, 374, 376, 378. The second embodiment 360 of the
26 flicker filter device 104 is shown coupled to a plurality of data

1 packers 202a, 202b, a plurality of data unpackers 204a, 204b,
2 204c, the first line buffer 108 and the second line buffer 110.

3 The color space converter 350 is coupled to the data source
4 102 to receive an RGB signal. The color space converter 350
5 preferably converts 24 bits of RGB to 24 bits in YCrCb format.
6 This conversion is done in a conventional manner. The output of
7 the color space converter 350 is coupled to the input of the 9-
8 tap chroma filter 352. The 9-tap chroma filter 352 performs
9 chroma filtering in a manner described above using the
10 coefficients uses coefficients of {3, 6, 8, 10, 10, 10, 8, 6, 3},
11 and scaling by 1/64, for example. The output of the 9-tap chroma
12 filter 352 is provided to an input of the first multiplexer 356,
13 to an input of the second multiplexer 358, to an input of the
14 flicker filter & aperture correction circuitry 354, and to an
15 input of the second data packer 202b.

16 The second multiplexer 358 also has a second input coupled
17 to the output of the data unpacker out 204. The control input is
18 coupled to receive a TVFF enable signal. Thus, the second
19 multiplexer 358 either outputs a flicker filtered signal from the
20 data unpacker out 204 or an signal that is not flicker filtered
21 directly from the output of the 9-tap chroma filter 352.

22 The first multiplexer 356 has its first input coupled to the
23 output of the 9-tap chroma filter 352, as described above, and a
24 second output coupled to the output of the flicker filter &
25 aperture correction circuitry 354. The first multiplexer 356
26 provides at its output either the new in coming data line or data
27 from the flicker filter & aperture correction circuitry 354. The

1 output of the first multiplexer 356 is in turn coupled to the
2 first data packer 202a which packs the data for storage in the
3 first line buffer 108. The first data packer 202a operates
4 similar to device 202 described above. The first data packer has
5 an input coupled to the output of the first multiplexer 356 and
6 an output coupled to an input of the first line buffer 108.

7 The first line buffer 108 is used to store data that has
8 been partially flicker filtered, and partial sums. The output of
9 the first line buffer 108 is coupled to an input of the data
10 unpacker out 204a to send data to the TV encoder 106. The output
11 of the first line buffer 108 is also coupled to an input of the
12 data unpacker 1 204a to send data to the flicker filter &
13 aperture correction circuitry 354.

14 The data packer 2 202b, the second line buffer 110, and the
15 data unpacker 2 204c are coupled together like their counter
16 parts the data packer 1 202a, the first line buffer 108, and the
17 data unpacker 1 204b. However, the input to the data packer 2
18 202b is coupled to the output of the 9-tap chroma filter 352 as
19 noted above, and the output of the data unpacker 2 204c is
20 coupled to a different output of the flicker filter & aperture
21 correction circuitry 354.

22 Finally, the second embodiment 360 provides similar control
23 logic including a line buffer (LB) write control unit 370, a LB
24 read control unit 372, a clock generator 374 which is a division
25 circuit for generating the FODCLK signal, a horizontal sync
26 control unit 376, and a vertical sync control unit 378. Based on
27 the timing diagrams that will be described, those skilled in the

1 art will understand how to construct these control units and how
 2 they operated to control the other components shown in Figure 3B.

3 FIGS. 4-8 illustrate various methods of operating the
 4 flicker filter device 104 of Figure 3A. FIGS. 4-7 illustrate
 5 production of interlaced output data from non-interlaced input
 6 data; while Figure 8 illustrates the production of output control
 7 signals from input control signals.

8 Figures 4A and 4B are timing diagrams illustrating a method
 9 for 2-tap flicker filtering utilizing the flicker filter device
 10 104 of Figure 3A. Figure 4A illustrates the production of an
 11 even field of an interlaced output which displays a total of 480
 12 lines; while Figure 4B illustrates the production of the
 13 corresponding odd field. The method is not limited to displays
 14 of 480 lines. Line buffer 110 is not required for 2-tap
 15 filtering.

16 The nomenclature used in FIGS. 4A and 4B is as follows. The
 17 signals FIODDF, FIVSYNC, . . . FOVSYNC are as described
 18 previously with respect to Figure 3A. The nomenclature "Ln"
 19 represents input data line n. Thus, in the 480-line example of
 20 FIGS. 4A and 4B, one frame of non-interlaced input data is
 21 represented by L0, L1, . . . L479, as illustrated in the row
 22 corresponding to FID[23:0]. The nomenclature "Lm, n" represents
 23 the data line which results from filtering input data lines m and
 24 n together. The output data lines are L0, 1; L2, 3; . . . L478,
 25 479 for the even field of Figure 4A and L1, 2; L3, 4; . . . L477,
 26 478; L479' for the odd field of Figure 4B, as illustrated in the
 27 rows corresponding to FOD[23:0].

Figure 4A illustrates production of the even field. Line 0 (L0) is received 400 by the flicker filter device 104 and written 402 to line buffer 108. When line 1 (L1) is received 404, line 0 is read 406 from line buffer 108 and then filtered with line 1. The filtered line L0, 1 is written 408 back to line buffer 108. This is basically a read-modify-write operation for line buffer 108. When the filtered data L0, 1 is written 408 to line buffer 108, it is read 410 from line buffer 108 and outputted 412 at half the clock rate at which input data is received. The same process is repeated for successive lines to produce the even field.

In more detail, referring additionally to Figure 3A, line 0 is received 400 by the input register 306, converted to the external 4:4:4 YCrCb format by the color space converter 308, and then converted from the external format to the internal format and written 402 to line buffer 108 by the data packer 202 under control of the write control circuit 302. Line 1 is then received 404 by the input register 306 and converted to external format by the color space converter 308. Simultaneously, line 0 is read 406 from buffer 108 and converted to external format by the data unpacker 204 under control of the read control circuit 304. Lines 0 and 1, both in external format, are then combined into filtered line L0,1 by filter circuit 200. The filtered line L0,1 is converted to internal format and written 408 back to line buffer 108 by the data packer 202 under control of the write control circuit 302. The data unpacker 204 under control of the read control circuit 304 reads 410 the filtered data L0,1 from

1 line buffer 108, converts it to external format, and outputs 412
2 the filtered line L0,1 via the output control circuit 310.

3 One type of write 408 operation is performed to line buffer
4 108 but two different types of read operations are performed:
5 one to read 406 the previously stored line and one to read 410
6 the output line. The two read operations 406, 410 may be
7 implemented by using a line buffer 108 with two read ports. In
8 the preferred embodiment of Figure 3A, however, the two read
9 operations 406, 410 are time multiplexed using two read pointers
10 LB1RD and LB1RD1, with signal LB1RDSEL selecting which read
11 pointer is active. As a result, the line buffer 108 only
12 requires a single read port.

13 Furthermore, the first read pointer LB1RD and the write
14 pointer LB1WR are both reset by LB1RST, which in this embodiment
15 is generated in response to either FIHSYNC or the rising edge of
16 FIHDE. The second read pointer LB1RD1 has an independent reset
17 LB1RST1, which in this embodiment is generated once for every two
18 input lines because one output data line is generated for every
19 two input data lines. Since the reset signal LB1RST is sometimes
20 generated when LB1RD1 is still actively reading from line buffer
21 108, the reset LB1RST should not corrupt data in the line buffer
22 108.

23 In the remaining descriptions, the level of detail contained
24 in the previous three paragraphs will be omitted for clarity.

25 The odd field of Figure 4B is produced in an analogous
26 manner with the following special cases at the beginning and end
27 of the field. At the beginning of the field, line 0 (L0) is not

1 used. At the end of the field, the last interlaced output line
2 (L479') should be produced by filtering lines 479 and 480, but
3 line 480 does not exist. Hence, L479' is produced either by not
4 filtering line 479 or by filtering line 479 with itself. Other
5 approaches for handling these special cases will be apparent to
6 those of ordinary skill in the art depending on implementation.

7 Figures 5A and 5B are timing diagrams illustrating a method
8 for 3-tap flicker filtering utilizing the flicker filter device
9 104 of Figure 3A. As with FIGS. 4A and 4B, Figure 5A illustrates
10 the production of an even field of an interlaced format
11 displaying 480 lines; while Figure 5B illustrates the production
12 of the corresponding odd field.

13 Basic operation is illustrated by the production of filtered
14 line L0,1,2 in Figure 5B. When line 0 (L0) is received 500, it
15 is written 502 to line buffer 110. When line 1 (L1) is received
16 504, it is written 506 to line buffer 108. When line 2 (L2) is
17 received 508, L0 is read 510 from line buffer 110 and L1 is read
18 512 from line buffer 108. All three lines L0, L1, and L2 are
19 filtered together and the resulting filtered line L0,1,2 is then
20 written 514 back into line buffer 108. When the filtered data
21 L0,1,2 is written 514 to line buffer 108, it is then read 516
22 from line buffer 108 and outputted 518 at half the input clock
23 rate. Line 2 is also written 520 to line buffer 110 in
24 preparation for the production of filtered line L2,3,4. The same
25 process is repeated for successive lines.

1 The read pointer LB2RD and write pointer LB2WR are cleared
2 by LB2RST, which in this embodiment is generated in response to
3 either FIHSYNC or the rising edge of FIHDE.

4 Special cases may occur at the beginning and end of each
5 field. For example, for the even field of Figure 5A, filtered
6 line L0,1 is a special case since line -1 does not exist. As
7 another example, for the odd field of Figure 5B, filtered line
8 L478,479 is a special case since line 480 does not exist. As
9 described previously, various approaches are generally known for
10 handling these special cases.

11 FIGS. 6A and 6B are timing diagrams illustrating a second
12 method for 3-tap flicker filtering utilizing the flicker filter
13 device 104 of Figure 3A. As usual, Figure 6A shows production of
14 the even field; while Figure 6B shows production of the odd
15 field.

16 Basic operation is illustrated by the production of filtered
17 line L0,1,2 in Figure 6B. Line 0 (L0) is received 600 and
18 written 602 to line buffer 110. When line 1 (L1) is received
19 604, line 0 is read 606 from line buffer 110 and filtered with
20 line 1. The resulting filtered line L0,1, which is an
21 intermediate result, is written 608 to line buffer 108. When
22 line 2 (L2) is received 610, intermediate result L0,1 is read 612
23 from line buffer 108 and filtered with line 2. The filtered line
24 L0,1,2 is then written 614 back to line buffer 108. When the
25 filtered data L0,1,2 is written 614 to line buffer 108, it is
26 then read 616 from line buffer 108 and outputted 618 at half the
27 input clock rate. Line 2 is also written 620 to line buffer 110

1 in preparation for the production of filtered line L2,3,4. The
2 same process is repeated for successive lines.

3 Again, special cases may occur at the beginning and/or end
4 of each field. Examples include filtered line L0,1 in Figure 6A
5 and filtered line L478,479 in Figure 6B.

6 FIGS. 7A and 7B are timing diagrams illustrating a third
7 method for 3-tap flicker filtering utilizing the flicker filter
8 device 104 of Figure 3A. As usual, Figure 7A shows production of
9 the even field; while Figure 7B shows production of the odd
10 field.

11 Basic operation is illustrated by the production of filtered
12 line L0,1,2 in Figure 7B. Line 0 (L0) is received 700 and
13 written 702 to line buffer 108. When line 1 (L1) is received
14 704, line 0 is read 706 from line buffer 108 and filtered with
15 line 1. The resulting filtered line L0,1, which is an
16 intermediate result, is written 708 to line buffer 108. When
17 line 2 (L2) is received 710, intermediate result L0,1 is read 712
18 from line buffer 108 and filtered with line 2. The filtered line
19 L0,1,2 is then written 714 to line buffer 110. When the filtered
20 data L0,1,2 is written 714 to line buffer 110, it is then read
21 716 from line buffer 110 and outputted 718 at half the input
22 clock rate. Line 2 is also written 720 to line buffer 108 in
23 preparation for the production of filtered line L2,3,4. The same
24 process is repeated for successive lines. Again, special cases
25 may occur at the beginning and/or end of each field. This method
26 has an advantage of not requiring the second read pointer LB1RD1
27 for line buffer 108.

1 The flicker filter device 104 of Figure 3A may implement any
2 of the 2-tap or 3-tap flicker filtering methods illustrated
3 above. Hence, one advantage of the flicker filter device 104 of
4 Figure 3A is that the same hardware may be used to implement
5 different flicker filter functions with different numbers of
6 taps.

7 FIGURE 8 is a timing diagram illustrating the production
8 of output control signals from input control signals, utilizing
9 the flicker filter device 104 of FIGURE 3. More specifically,
10 the output control circuit 310 generates the interlaced output
11 control signals FOHSYNC, FODE, and FOVSYNC from the non-
12 interlaced mode input control signals FIHSYNC, FIHDE, FIVDE,
13 FIVBLANK, and FIVSYNC. As a result of the conversion from non-
14 interlaced format to interlaced format, input data is received at
15 twice the rate at which output data is generated.

16 In the preferred embodiment of Figure 8, the generation of
17 output control signals is initiated at the beginning of the even
18 field. Figure 8 depicts a time period corresponding to this
19 initiation.

20 FOHSYNC is generated as follows. The portion of the output
21 control circuit 310 that generates FOHSYNC is reset at the first
22 rising edge 800 of horizontal display enable (FIHDE) that follows
23 the falling edge 802 of vertical blank (FIVBLANK) during even
24 field (i.e., FIODDF is low 804). Reset does not occur during odd
25 fields. The output control circuit 310 determines the start
26 position T1 of FIHSYNC, which is the time between the rising edge
27 800 of FIHDE and the rising edge 806 of FIHSYNC. The output

1 control circuit 310 also determines the width T2 of FIHSYNC.
2 Both T1 and T2 are multiplied by two to generate the interlaced
3 horizontal sync output FOHSYNC, which is referenced to the
4 leading edge 800 of FIHDE. The flicker filter data pipeline
5 delay is also added in generation of FOHSYNC. In Figure 8,
6 Latency is provide to match the delay through the flicker filter
7 device 200 and the delay in processing the data in the color
8 space converter 308.

9 FODE is generated by determining the period T3 from the
10 falling edge 812 of FIHSYNC to the next leading edge 814 of
11 FIHDE. The parameters T1, T2, and T3, are all multiplied by two
12 to produce the interlaced output enable FODE, also referenced to
13 the leading edge 800 of FIHDE.

14 In the embodiment of Figure 8, the generation of FOHSYNC and
15 starts one line earlier from the first active input line (L0) or
16 two lines earlier from the first active output data (L0,1) and
17 output display enable (FODE). This results in the correct
18 synchronization of FOHSYNC with FODE and FOD[23:0]. In general,
19 generation of FOHSYNC must begin at a point which ensures that
20 FOHSYNC will be generated in between two output lines.

21 FOVSYNC is generated by delaying FIVSYNC by the flicker
22 filter data pipeline delay and also by the amount specified in TV
23 VSYNC delay register (SR78). A counter which is used to delay
24 both the rising edge and the falling edge of FIVSYNC by the
25 amount specified by SR78 is incremented by FFCLK/16. Because the
26 vertical sync can be delayed by more than one horizontal time,
27 FIVSYNC can be optionally programmed such that it is generated

1 one line earlier than shown in the above timing diagrams and then
2 delayed by approximately one horizontal time. This is highly
3 recommended because FOVSYNC can then be positioned independently
4 of FOHSYNC. The delay depends on timing based on the programming
5 of the CRT controller.

6 Although the invention has been described in considerable
7 detail with reference to certain preferred embodiments thereof,
8 other embodiments are possible. For example, the invention can
9 be incorporated into an integrated circuit on a semiconductor
10 device using techniques known in the art. Therefore, the spirit
11 and scope of the appended claims should not be limited to the
12 description of the preferred embodiments contained herein.

WHAT IS CLAIMED IS:

1 1. A device for flicker filtering a plurality of non-
2 interlaced lines containing computer graphics data to form a
3 plurality of interlaced lines, the device programmable to combine
4 either two or three non-interlaced lines to form each interlaced
5 line, the device comprising:

6 a data packer having an input and two outputs for converting
7 data from an external format to an internal format, the
8 two outputs adapted to write data in the internal
9 format to a first line buffer and to a second line
10 buffer respectively;

11 a data unpacker having two inputs and two outputs for
12 converting data read from the first and second line
13 buffers from the internal format to the external
14 format, the two inputs adapted to receive data read
15 from the first line buffer and from the second line
16 buffer respectively, the first output adapted to output
17 data in the external format; and

18 a filter circuit having two inputs and an output for
19 combining data received at the two inputs into filtered
20 data, the first input adapted to receive data
21 containing video information in the external format,
22 the second input coupled to receive data from the
23 second output of the data unpacker, the output coupled
24 to send the filtered data in the external format to the
25 input of the data packer.

1 2. The device of claim 1 wherein:

2 the data packer further has a second input adapted to
3 receive data containing computer graphics in the
4 external format.

1 3. The device of claim 1 further comprising:

2 a line buffer write control circuit, adapted to receive an
3 external control signal including a clock, adapted to
4 send a line buffer write control signal to the first
5 and second line buffers, and coupled to send a data
6 packer control signal to the data packer, for
7 generating the line buffer write control signal and the
8 data packer control signal in response to the external
9 control signal; and

10 a line buffer read control circuit, adapted to receive the
11 external control signal, adapted to send a line buffer
12 read control signal to the first and second line
13 buffers, and coupled to send a data unpacker control
14 signal to the data unpacker, for generating the line
15 buffer read control signal and the data unpacker
16 control signal in response to the external control
17 signal.

1 4. The device of claim 3 wherein the line buffer read
2 control signal comprises:

3 a first read pulse for reading from the first line buffer;
4 and

a second read pulse for reading from the first line buffer.

5. The device of claim 4 wherein:

a first read pulse increments a first pointer to the first
line buffer; and
the second read pulse increments a second pointer to the
first line buffer.

6. The device of claim 1 comprising:

a color space converter adapted to receive data in a second
external format, for converting the data from the
second external format to the external format.

7. The device of claim 6 wherein:

the second external format is an RGB format; and
the external format is a 4:4:4 signed YCrCb format.

8. The device of claim 1 wherein:

the external format is a 4:4:4 signed YCrCb format.

9. The device of claim 8 wherein:

the internal format is programmably selected from a group
consisting of a 4:4:4 YCrCb format, a 4:2:2 YCrCb
format, and a 4:1:1 YCrCb format.

10. The device of claim 1 further comprising:

an output control circuit adapted to receive a non-
interlaced mode control signal and adapted to send an
interlaced mode control signal, for converting the non-

interlaced mode control signal to the interlaced mode control signal.

11. The device of claim 10 wherein the non-interlaced mode control signal includes a first horizontal sync signal, a first vertical sync signal, a vertical blank signal, and a horizontal blank signal; and the interlaced mode control signal includes a second horizontal sync signal, a second vertical sync signal, and a blank signal.

12. A method for flicker filtering a plurality of non-interlaced lines to form a plurality of interlaced lines, the method comprising the steps of:

- receiving a non-interlaced line in an external format;
- converting the received non-interlaced line from the external format to an internal format;
- retrieving an intermediate line in the internal format from a line buffer;
- combining the non-interlaced and intermediate lines to form a filtered line in the internal format; and
- converting the filtered line from the internal format to the external format to form an interlaced line.

13. The method of claim 12 wherein the external format is a 4:4:4 signed YCrCb format.

14. The method of claim 13 further comprising the step of:

selecting the internal format from a group consisting of a 4:4:4 YCrCb format, a 4:2:2 YCrCb format, and a 4:1:1 YCrCb format.

15. A method for flicker filtering a plurality of non-interlaced lines to form a plurality of interlaced lines, each interlaced line formed from two non-interlaced lines, the method utilizing a line buffer and comprising the steps of:

receiving a first non-interlaced line and writing said line to a line buffer;

simultaneously reading the first non-interlaced line from the line buffer, receiving a second non-interlaced line, combining the first and second non-interlaced lines to form an interlaced line, and writing the interlaced line to the line buffer; and

repeating the above steps to form a plurality of interlaced lines.

16. A method for flicker filtering a plurality of non-interlaced lines to form a plurality of interlaced lines, each interlaced line formed from three non-interlaced lines, the method utilizing two line buffers and comprising the steps of:

receiving a first non-interlaced line and writing said line to a first line buffer;

simultaneously reading the first non-interlaced line from the first line buffer, reading a second non-interlaced line from a second line buffer, receiving a third non-interlaced line and writing said line to the second

11 line buffer, combining the first, second and third non-
12 interlaced lines to form an interlaced line, and
13 writing the interlaced line to the first line buffer;
14 and
15 repeating the above steps to form a plurality of interlaced
16 lines.

1 17. A method for flicker filtering a plurality of non-
2 interlaced lines to form a plurality of interlaced lines, each
3 interlaced line formed from three non-interlaced lines, the
4 method utilizing two line buffers and comprising the steps of:
5 simultaneously reading a first non-interlaced line from a
6 first line buffer, receiving a second non-interlaced
7 line, combining the first and second non-interlaced
8 lines to form an intermediate line, and writing the
9 intermediate line to a second line buffer;
10 simultaneously reading the intermediate line from the second
11 line buffer, receiving a third non-interlaced line and
12 writing said line to the first line buffer, combining
13 the intermediate and third non-interlaced lines to form
14 an interlaced line, and writing the interlaced line to
15 the second line buffer; and
16 repeating the above steps to form a plurality of interlaced
17 lines.

1 18. A method for flicker filtering a plurality of non-
2 interlaced lines to form a plurality of interlaced lines, each

interlaced line formed from three non-interlaced lines, the method utilizing two line buffers and comprising the steps of:

simultaneously reading a first non-interlaced line from a first line buffer, receiving a second non-interlaced line, combining the first and second non-interlaced lines to form an intermediate line, and writing the intermediate line to the first line buffer;

simultaneously reading the intermediate line from the first line buffer, receiving a third non-interlaced line and writing said line to the first line buffer, combining the intermediate and third non-interlaced lines to form an interlaced line, and writing the interlaced line to a second line buffer; and

repeating the above steps to form a plurality of interlaced lines.

1 SYSTEM AND METHODS FOR 2-TAP / 3-TAP FLICKER FILTERING

2
3 ABSTRACT OF THE DISCLOSURE

4 A device performs both 2-tap and 3-tap flicker filtering of
5 non-interlaced lines of computer graphics data to form interlaced
6 lines. The device includes a data packer, a data unpacker, and a
7 filter circuit. The filter circuit combines lines that it
8 receives to form filtered lines. The data packer writes the
9 filtered lines to line buffers while the data unpacker reads the
10 lines stored in the line buffers. The read lines are either sent
11 to the filter circuit for further filtering or are outputted to
12 be displayed as interlaced lines. Both 2-tap and 3-tap flicker
13 filtering can be accomplished by varying the order and/or number
14 of read, write, and filter operations.

0010/PTO Rev. 6/95	U.S. Department of Commerce Patent and Trademark Office	Attorney Docket Number 2723	
DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION		First Named Inventor Reena Premi	
		COMPLETE IF KNOWN	
		Application Number Not yet assigned	
		Filing Date On Even Date Herewith	
		Group Art Unit Unknown	
		Examiner Name Unknown	
<div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> <input checked="" type="checkbox"/> Declaration Submitted with Initial Filing </div> <div style="width: 10%; text-align: center;">OR</div> <div style="width: 45%;"> <input type="checkbox"/> Declaration Submitted after Initial Filing </div> </div>			

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

SYSTEM AND METHODS FOR 2-TAP / 3-TAP FLICKER FILTERING

the specification of which

(Title of the Invention)

☒ is attached hereto

OR

☐ was filed on (MM/DD/YYYY) [] as United States Application Number or PCT International Application Number [] and was amended on (MM/DD/YYYY) [] (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37 Code of Federal Regulations. § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code § 119 (a)-(d) or § 385(b) of any foreign application(s) for patent or inventor's certificate, or § 365 (a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached?	
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

☐ Additional foreign application numbers are listed on a supplemental priority sheet attached hereto:

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Date (MM/DD/YYYY)	<input type="checkbox"/> Additional provisional application numbers are listed on a supplemental sheet attached hereto.

4677-229000

DECLARATION					ADDITIONAL INVENTOR(S) Supplemental Sheet			
Name of Additional Joint Inventor, if any:					<input type="checkbox"/> A petition has been filed for this unsigned inventor			
Given Name	William	Middle Initial	S.	Family Name	Herz	Suffix e.g. Jr.		
Inventor's Signature	William S. Herz				Date	11/11/97		
Residence: City	Newark	State	CA	Country	U.S.A.	Citizenship	U.S.A.	
Mailing Address	39708 Potrero Drive							
Mailing Address								
City	Newark	State	CA	Zip	94560	Country	U.S.A.	
Name of Additional Joint Inventor, if any:					<input type="checkbox"/> A petition has been filed for this unsigned inventor			
Given Name	Ignatius	Middle Initial	B.	Family Name	Tjandrasuwita	Suffix e.g. Jr.		
Inventor's Signature					Date			
Residence: City	Union City	State	CA	Country	U.S.A.	Citizenship	U.S.A.	
Mailing Address	32421 Seaside Drive							
Mailing Address								
City	Union City	State	CA	Zip	94587	Country	U.S.A.	
Name of Additional Joint Inventor, if any:					<input type="checkbox"/> A petition has been filed for this unsigned inventor			
Given Name		Middle Initial		Family Name		Suffix e.g. Jr.		
Inventor's Signature					Date			
Residence: City		State		Country		Citizenship		
Mailing Address								
Mailing Address								
City		State		Zip		Country		
Name of Additional Joint Inventor, if any:					<input type="checkbox"/> A petition has been filed for this unsigned inventor			
Given Name		Middle Initial		Family Name		Suffix e.g. Jr.		
Inventor's Signature					Date			
Residence: City		State		Country		Citizenship		
Mailing Address								
Mailing Address								
City		State		Zip		Country		

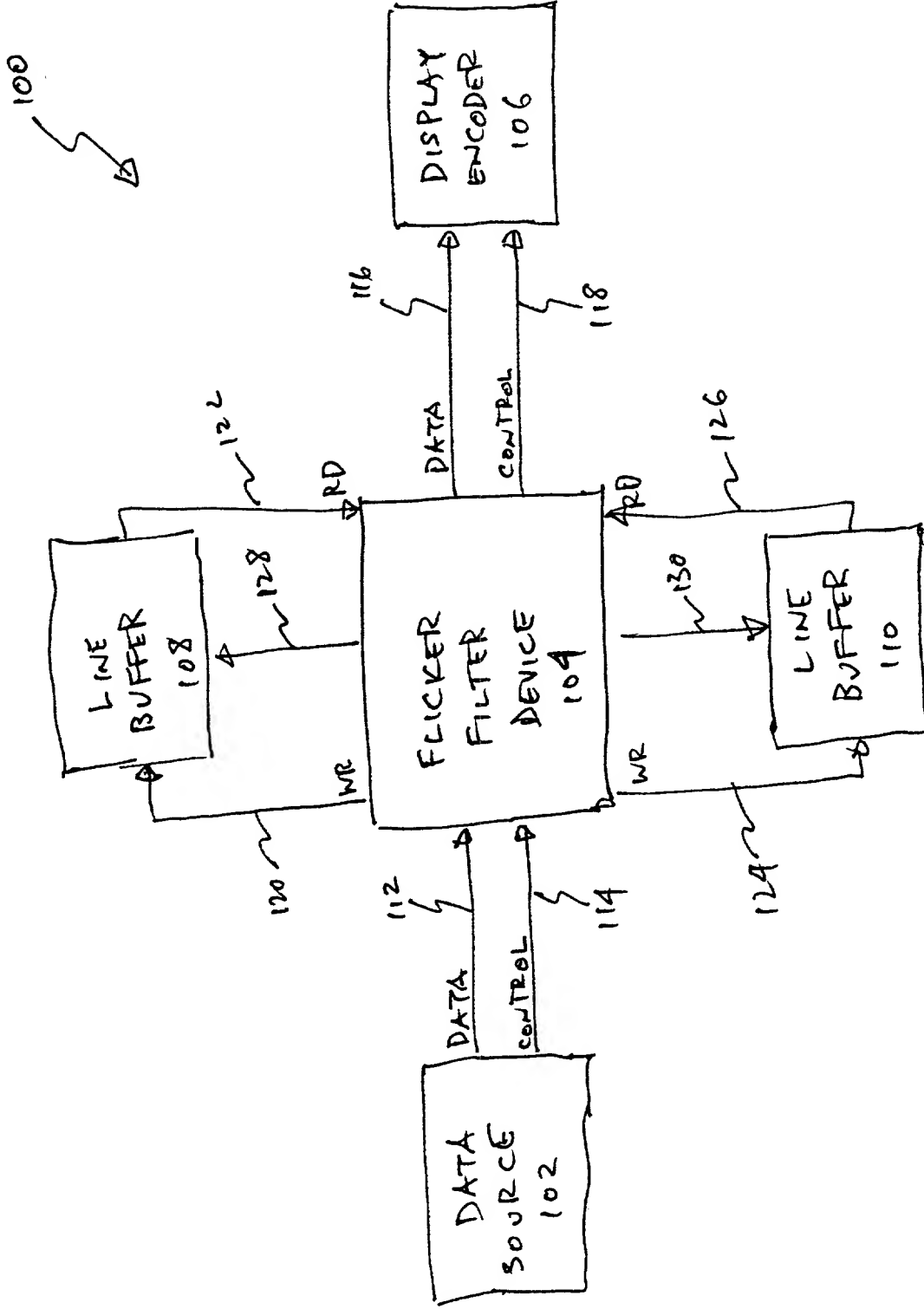


FIGURE 1

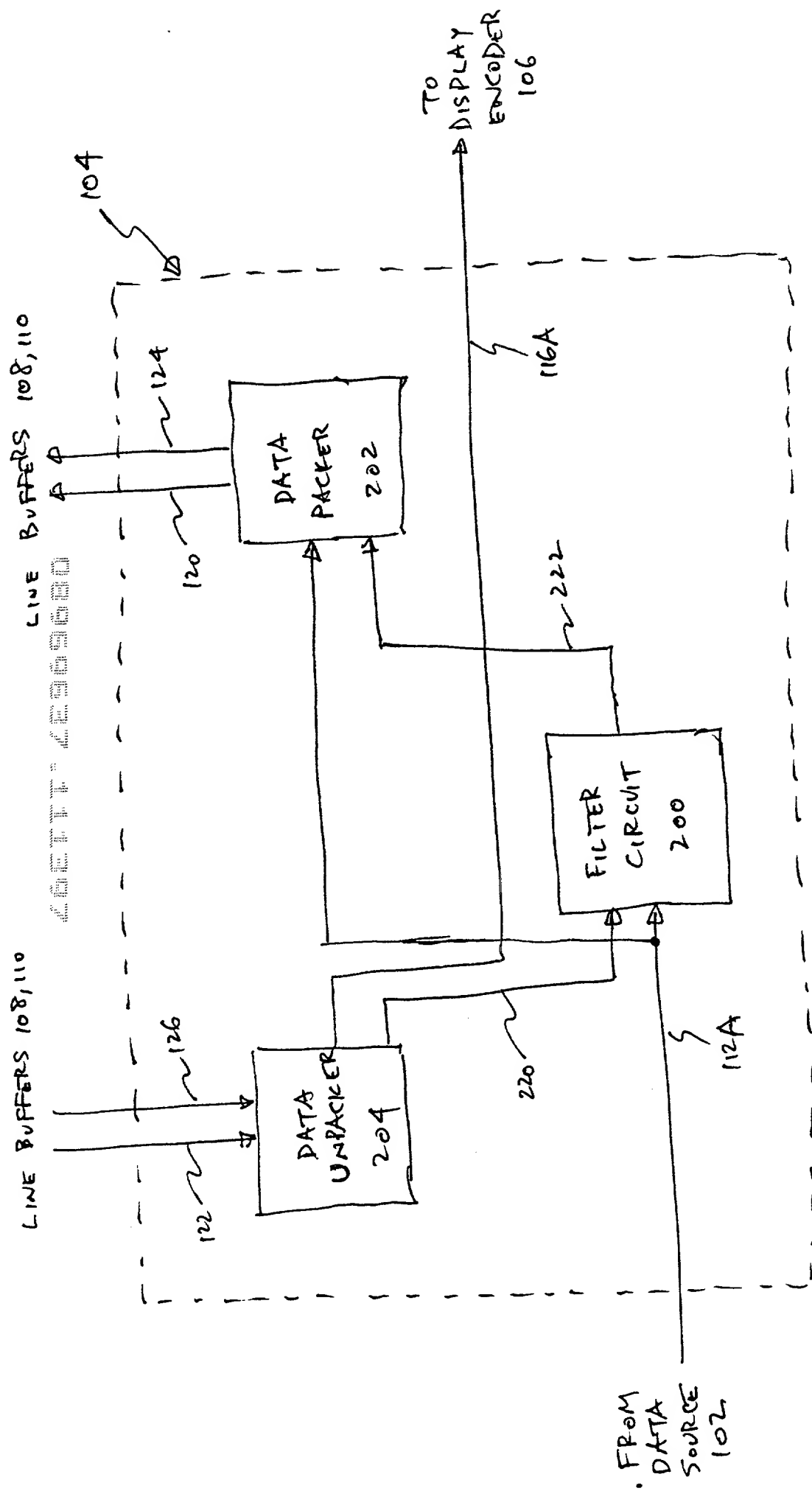


FIGURE 2

Parameter	Value	Unit
α	0.001	
β	0.001	
γ	0.001	
δ	0.001	
ϵ	0.001	
ζ	0.001	
η	0.001	
θ	0.001	
ι	0.001	
κ	0.001	
λ	0.001	
μ	0.001	
ν	0.001	
ξ	0.001	
\omicron	0.001	
π	0.001	
ρ	0.001	
σ	0.001	
τ	0.001	
υ	0.001	
ϕ	0.001	
χ	0.001	
ψ	0.001	
ω	0.001	
Ω	0.001	
Θ	0.001	
Υ	0.001	
Φ	0.001	
Ψ	0.001	
Ξ	0.001	
\Omicron	0.001	
Π	0.001	
Σ	0.001	
Υ	0.001	
Φ	0.001	
Ψ	0.001	
Ξ	0.001	
\Omicron	0.001	
Π	0.001	
Σ	0.001	
Υ	0.001	
Φ	0.001	
Ψ	0.001	
Ξ	0.001	
\Omicron	0.001	
Π	0.001	
Σ	0.001	
Υ	0.001	
Φ	0.001	
Ψ	0.001	
Ξ	0.001	
\Omicron	0.001	
Π	0.001	
Σ	0.001	
Υ	0.001	
Φ	0.001	
Ψ	0.001	
Ξ	0.001	
\Omicron	0.001	
Π	0.001	
Σ	0.001	
Υ	0.001	
Φ	0.001	
Ψ	0.001	
Ξ	0.001	
\Omicron	0.001	
Π	0.001	
Σ	0.001	
Υ	0.001	
Φ	0.001	
Ψ	0.001	
Ξ	0.001	
\Omicron	0.001	
Π	0.001	
Σ	0.001	
Υ	0.001	
Φ	0.001	
Ψ	0.001	
Ξ	0.001	
\Omicron	0.001	
Π	0.001	
Σ	0.001	
Υ	0.001	
Φ	0.001	
Ψ	0.001	
Ξ	0.001	
\Omicron	0.001	
Π	0.001	
Σ	0.001	
Υ	0.001	
Φ	0.001	
Ψ	0.001	
Ξ	0.001	
\Omicron	0.001	
Π	0.001	
Σ	0.001	
Υ	0.001	
Φ	0.001	
Ψ	0.001	
Ξ	0.001	
\Omicron	0.001	
Π	0.001	
Σ	0.001	
Υ	0.001	
Φ	0.001	
Ψ	0.001	
Ξ	0.001	
\Omicron	0.001	
Π	0.001	
Σ	0.001	
Υ	0.001	
Φ	0.001	
Ψ	0.001	
Ξ	0.001	
\Omicron	0.001	
Π	0.001	
Σ	0.001	
Υ	0.001	

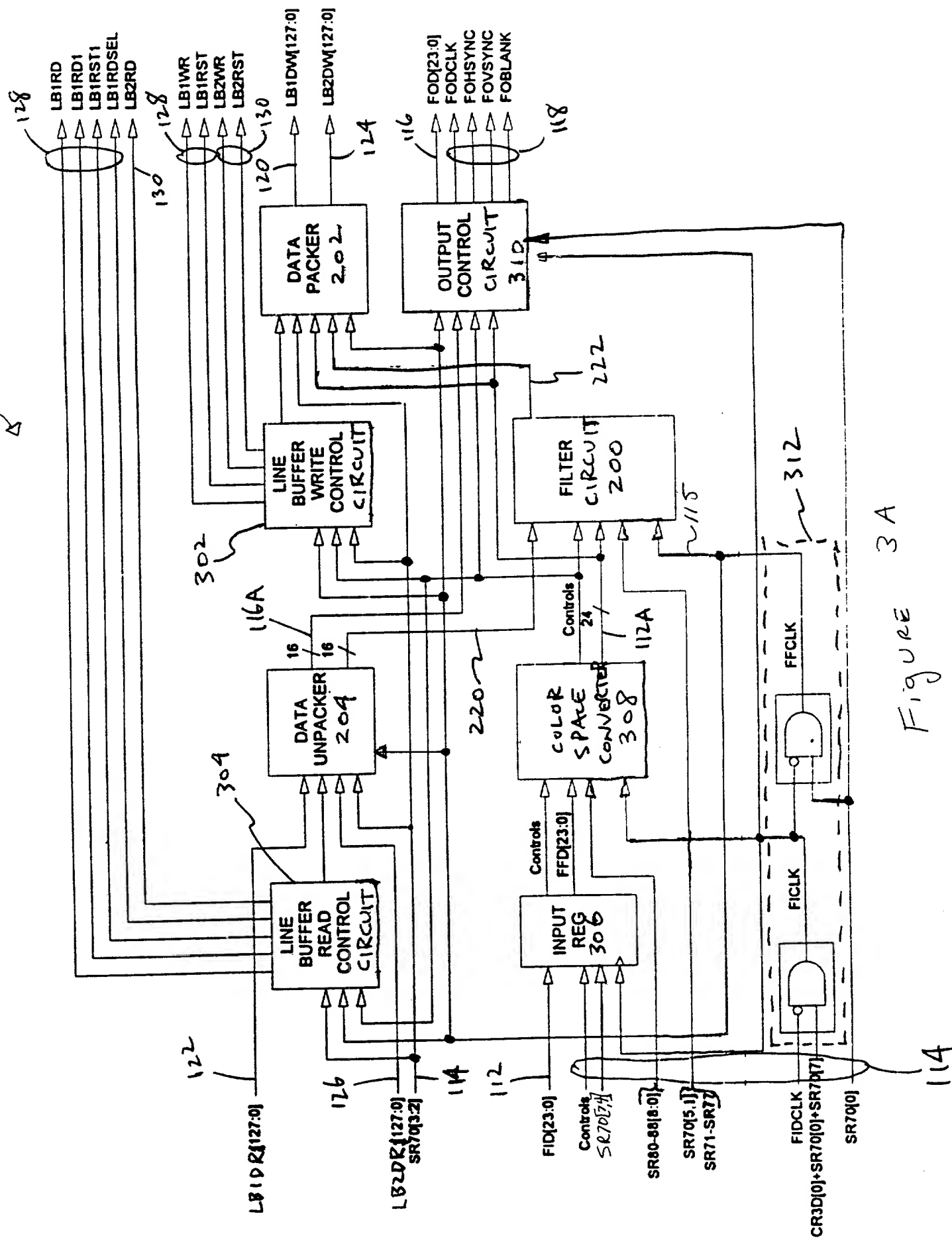


Figure 3A

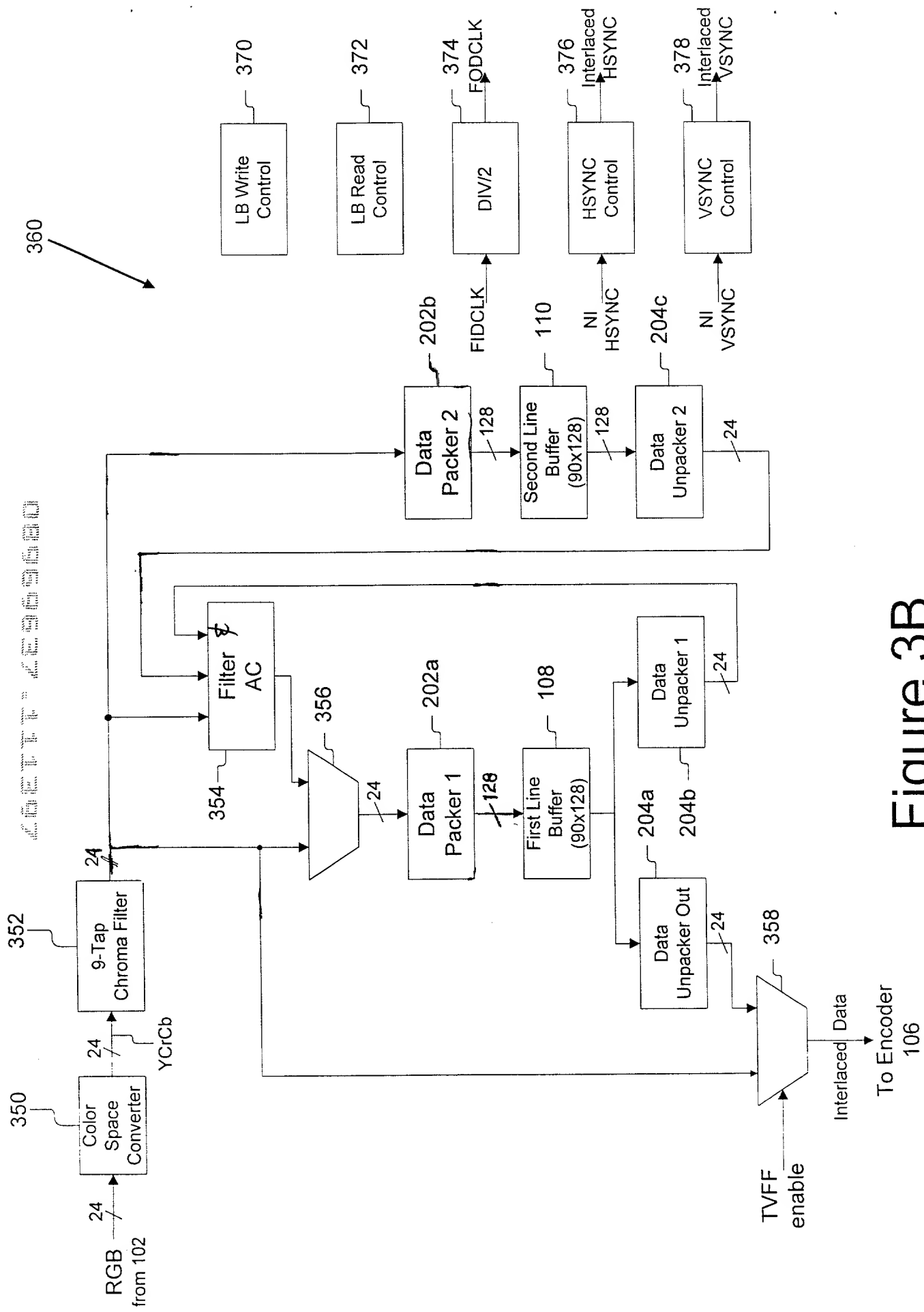


Figure 3B

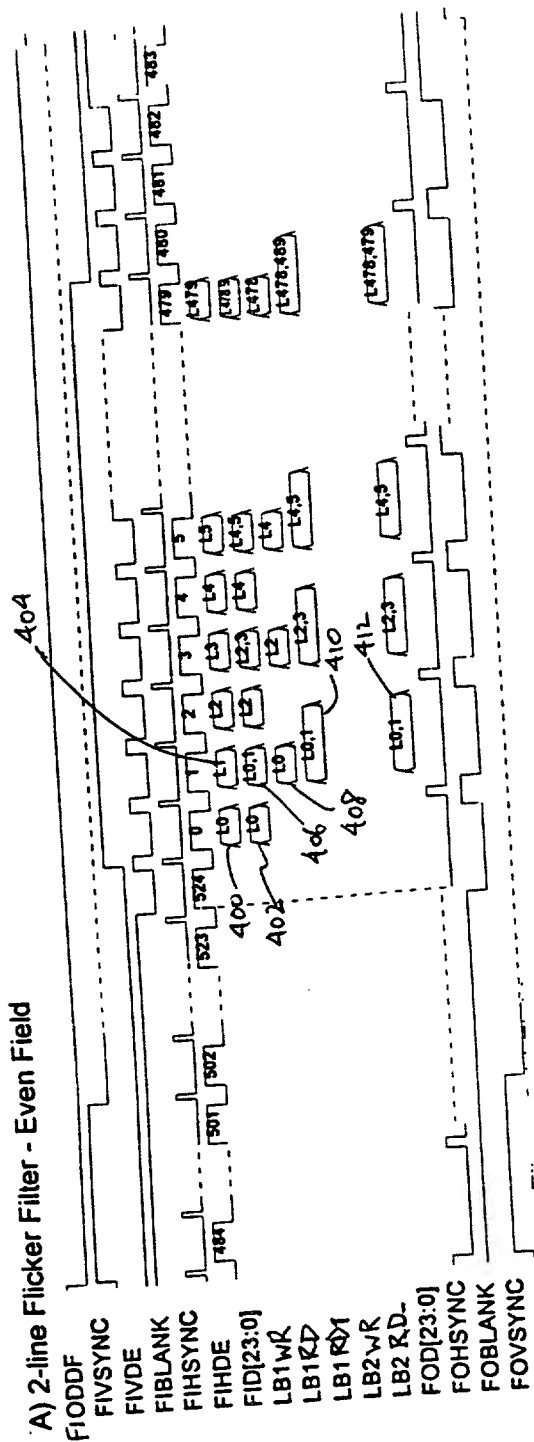


FIGURE 4A

[illegible]

FIGURE 4B

A) 3-line Flicker Filter - Even Field

Timing diagram for a 3-line Flicker Filter - Even Field. The diagram shows the relationship between various video signals and line numbers. The signals are: RODDF, FIVSYN, FIVDE, FIBLANK, FHSYN, FIHDE, FID[23:0], LB1wK, LB1RD, LB1RD1, LB2wR, LB2RD, FOD[23:0], FOHSYN, FOBLANK, and FOVSYN. The diagram is divided into two main sections by a dashed line. The top section shows the timing for lines 481 to 483, and the bottom section shows the timing for lines 479 to 477. The signals are represented by horizontal bars of different widths and positions, indicating their duration and timing relative to the lines.

FIGURE 5A

B) 3-line Flicker Filter - Odd Field

Timing diagram for 3-line Flicker Filter - Odd Field. The diagram shows horizontal sync pulses and various video signals. Handwritten annotations include 'S08' at the top, and various line numbers (500, 504, 506, 514, 516, 518, 520, 522, 524) and frame numbers (1, 2, 3, 4, 5) with arrows pointing to specific sync pulses. A list of signals is on the right: FIDODDF, FIVSYNC, FIVDE, FIBLANK, FIHSYNC, FIHDE, FID[23:0], LB1wR, LB1RD, LB1RD1, LB2wR, LB2RD, FOD[23:0], FOHSYNC, FOBLANK, FOVSYNCR, FOVSYNCR.

FIGURE SB

A) 3-line Flicker Filter - Even Field

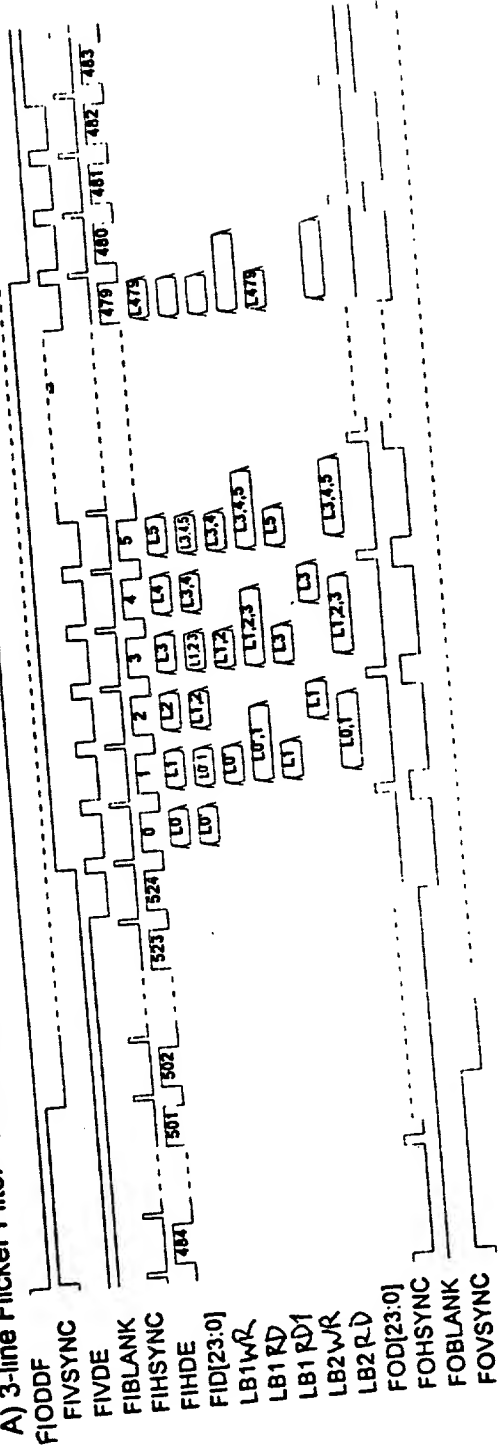


FIGURE 6A

B) 3-line Flicker Filter - Odd Field

FIGURE 6B

A) 3-line Flicker Filter - Even Field

Timing diagram for 3-line Flicker Filter - Even Field. The diagram shows horizontal sync pulses and various video signals. The signals are: F1ODDF, F1VSYNC, F1VDE, F1BLANK, F1HSYNC, F1HDE, F1D(23:0), LB1WR, LB1RD, LB1RD1, LB2WR, LB2RD, FOD(23:0), FOHSYNC, FOBLANK, and FOVSYNC. The diagram is divided into two main sections by a dashed line. The top section shows the first half of the frame, and the bottom section shows the second half. The signals are labeled with their respective line numbers and values.

Signal	Line 1	Line 2	Line 3	Line 4	Line 5
F1ODDF					
F1VSYNC					
F1VDE					
F1BLANK					
F1HSYNC					
F1HDE					
F1D(23:0)					
LB1WR					
LB1RD					
LB1RD1					
LB2WR					
LB2RD					
FOD(23:0)					
FOHSYNC					
FOBLANK					
FOVSYNC					

FIGURE 7A

[illegible]

FIGURE 7B

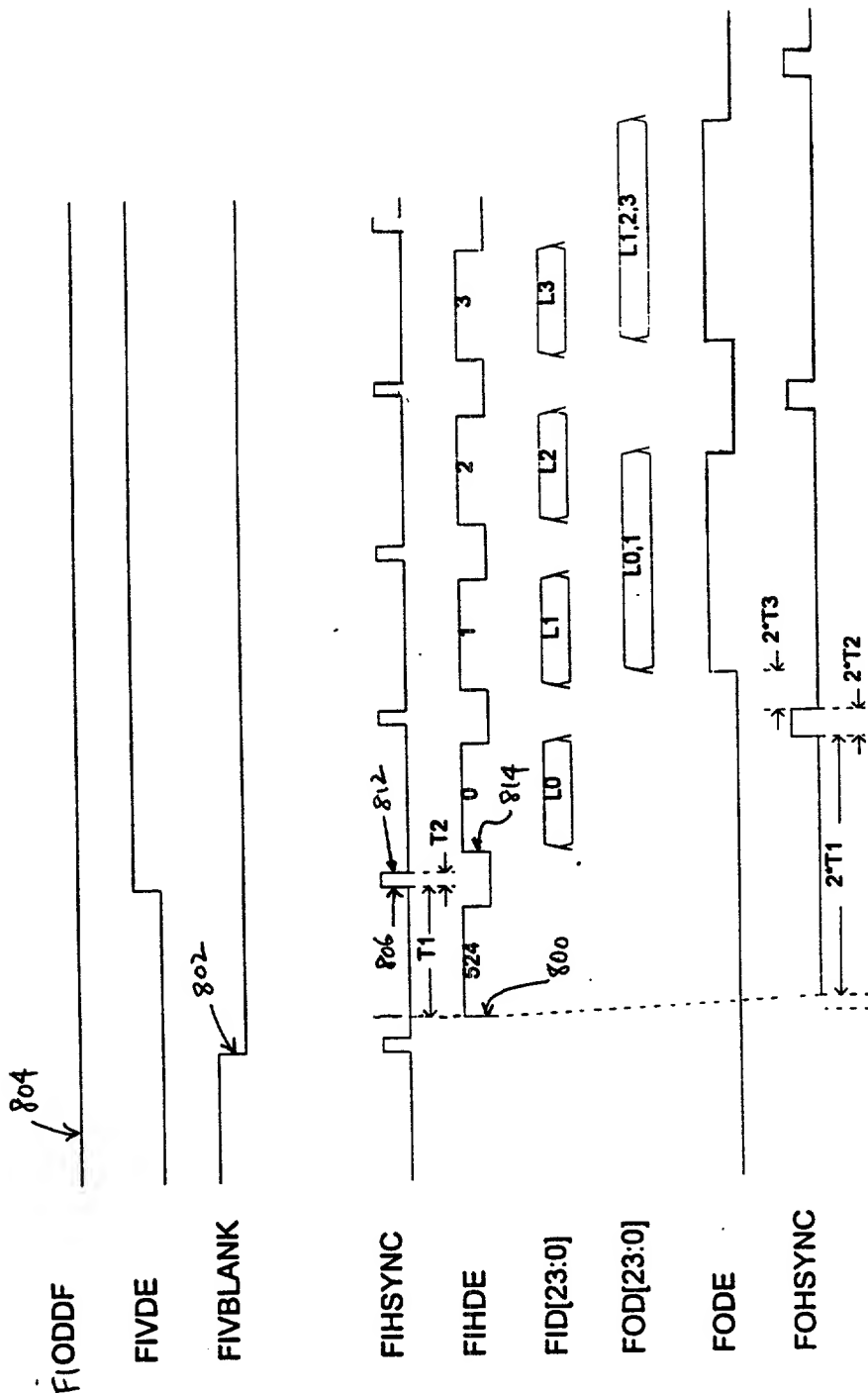


FIGURE 8